



# Total Ionizing Dose Effects on a CDTI based CCD-on-CMOS through Buildup of Interface Traps and Oxide Charges

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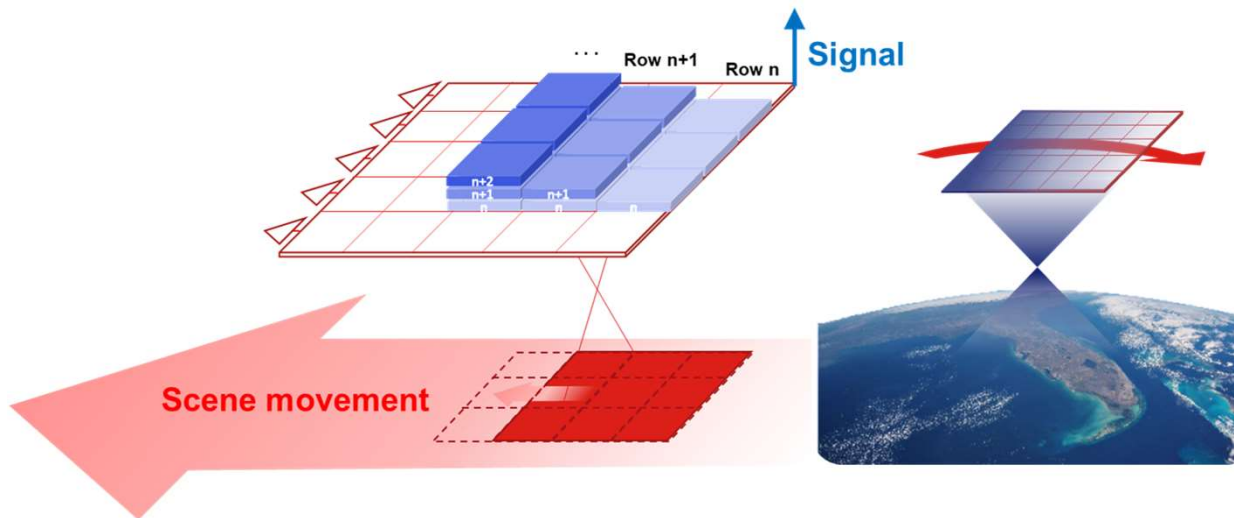




# 1 – Introduction

## Motivations for developing CCD-on-CMOS devices

- **CIS** : High-Tech manufacturing process, high level of integration, low voltages and radiation hardness.
- **Example** : High Resolution Earth imaging using Time Delay Integration (TDI)
- **CCD-on-CMOS** : Perform « CCD missions » requiring charge domain operations : transfer, binning, avalanche etc...
- **The Investigation of TID effects is beneficial for :**

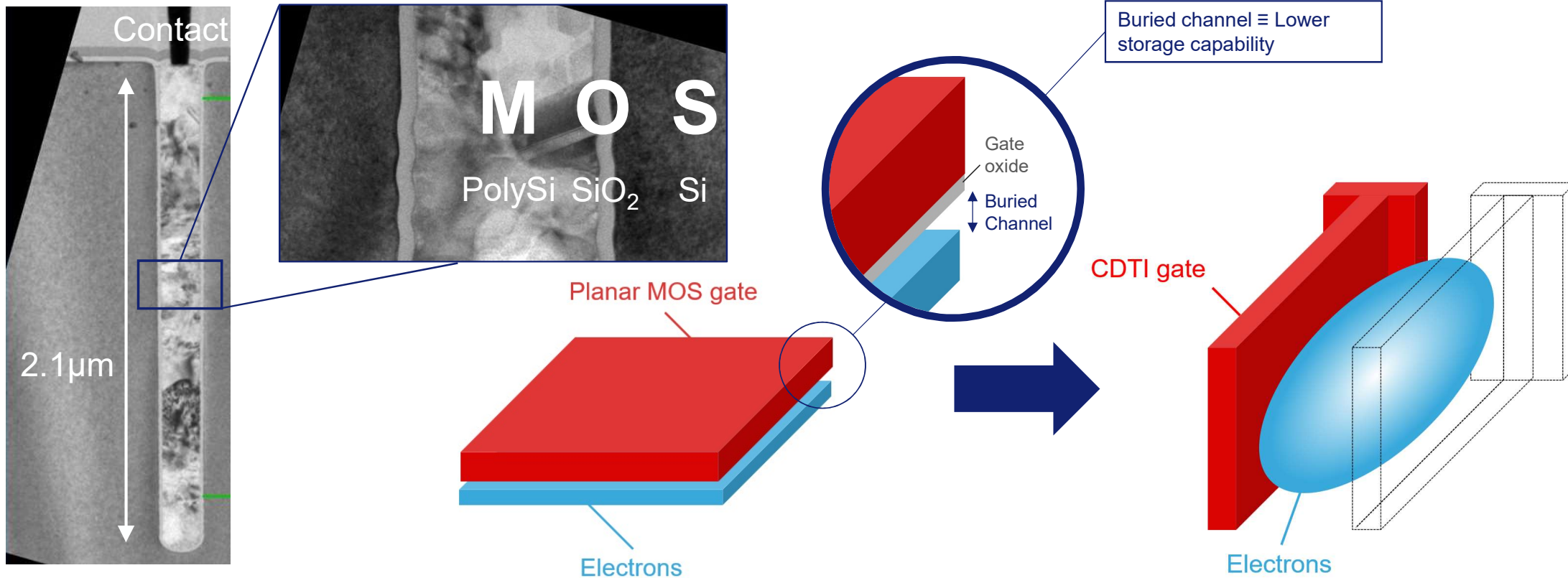


- Assessing Space environment compatibility,
- Improving the understanding of the device physical properties,
- Informing on the hardness of CDTI based structures.



## 2 – Device description

### Capacitive Deep Trench Isolation (CDTI)

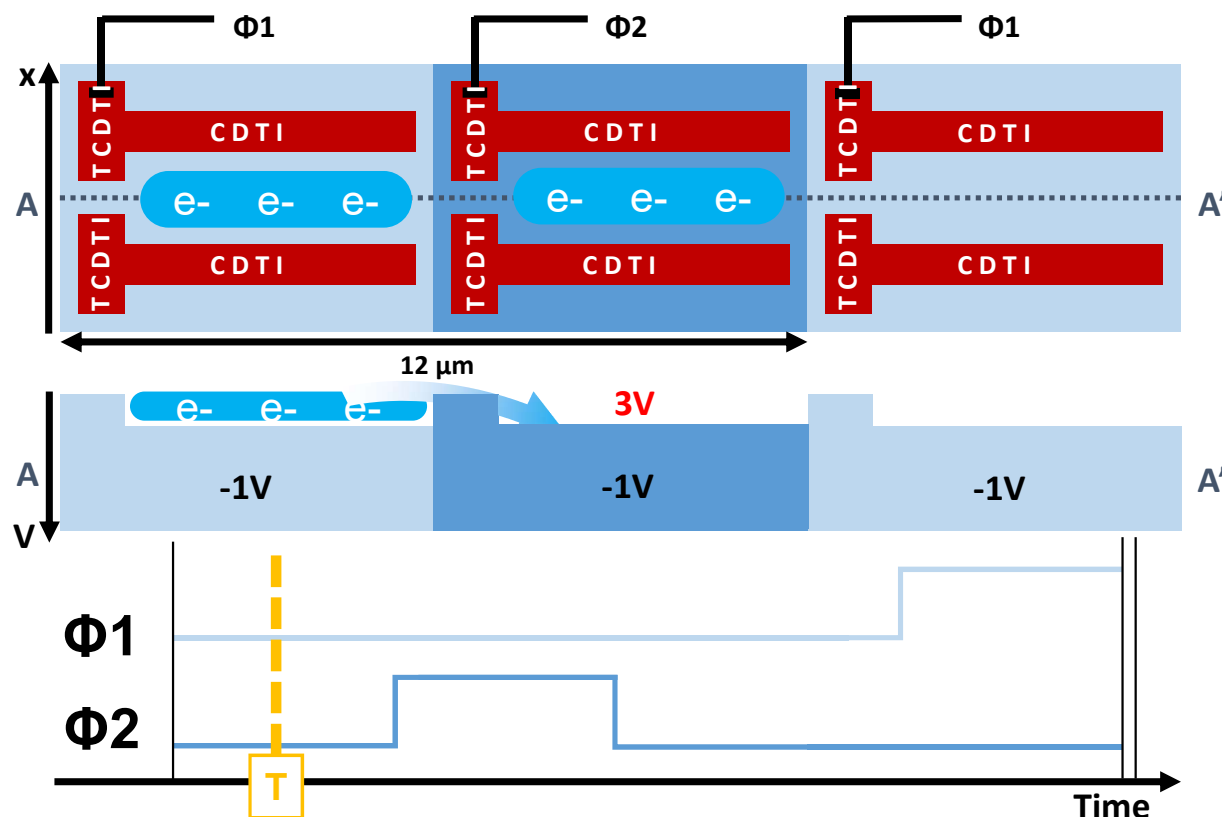


- Thanks to CDTIs the silicon bulk can be fully depleted by use of small voltages in a very large volume enhancing a large storage capability with electrical and optical crosstalks reduction.



## 2 – Device Description

### Charge Transfer Operation



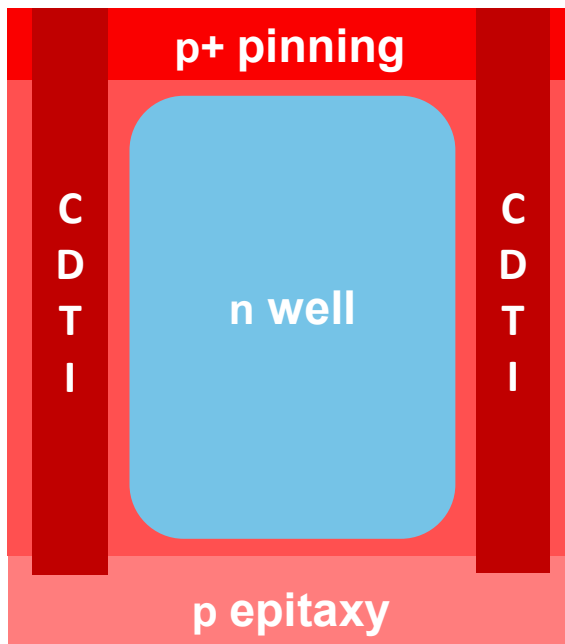
#### 2-Phase CCD :

- Low State : CDTI **inverted** → Low Dark current.
- High State : CDTI **depleted** → High Dark current.
- Short transfer time : Fully passivated → **Multi-Pinned Phase Mode (MPP)**.

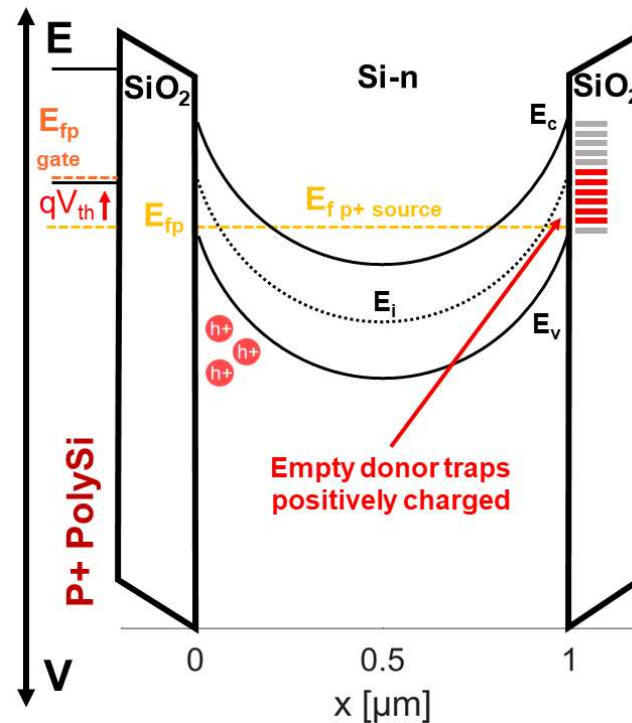
## 2 – Device Description

### Band Diagram under full depletion

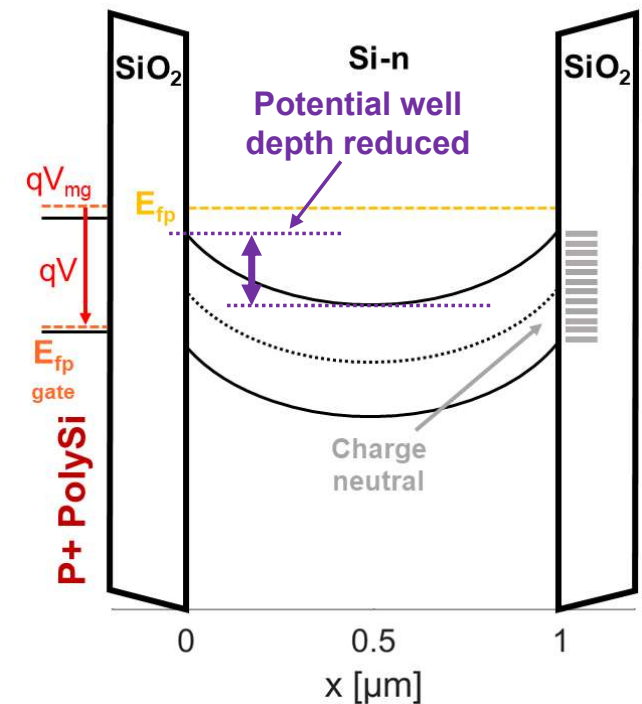
Cross-section view



Inversion



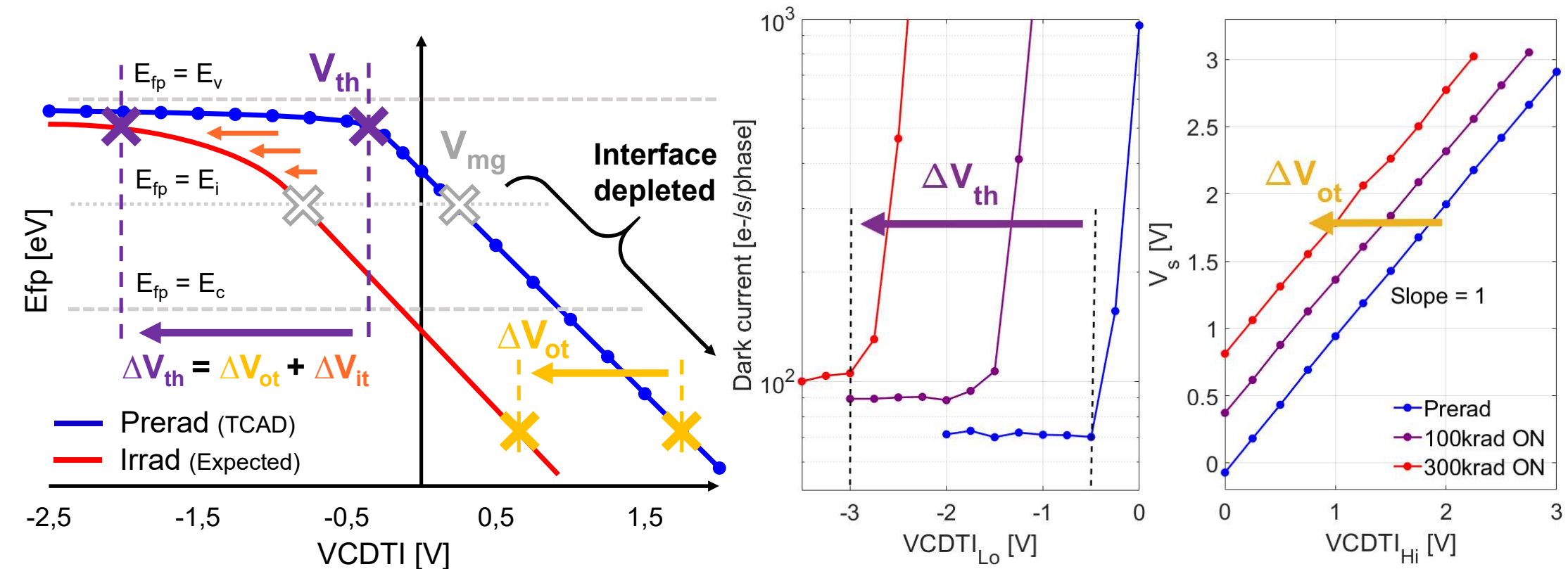
Depletion



- The CCD is operated with interfaces inverted during storage and depleted during transfer. As a consequence, the interface trapped charge only fully contribute to the threshold voltage at inversion.

## 2 – Device Description

$\Delta V_{ot}$  and  $\Delta V_{it}$  contributions and separation technique

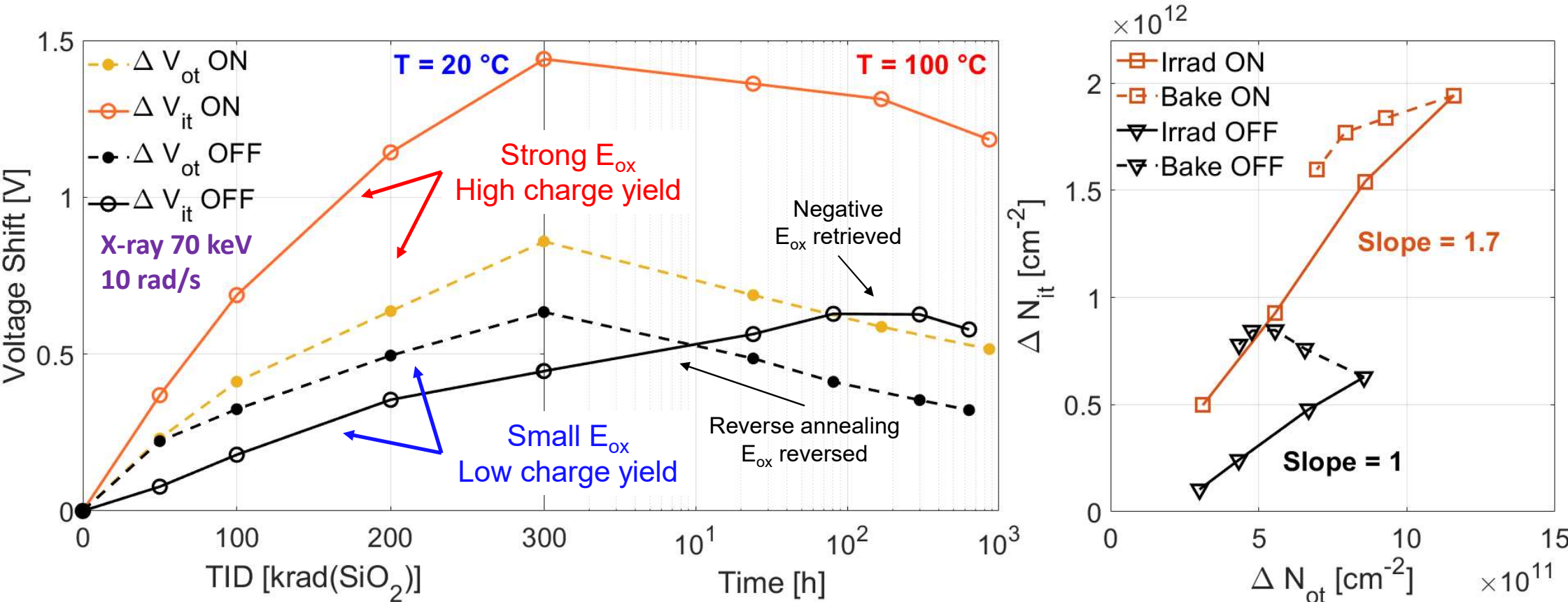


- The studied shifts are dominated by  $\Delta V_{ot}$  except when reaching inversion.  $\Delta V_{it}$  is derived by subtracting  $\Delta V_{ot}$  to the measured  $\Delta V_{th}$ .  $\Delta V_{ot}$  is obtained through potential barrier measurements under full depletion.



### 3 – Results

$\Delta V_{ot}$ ,  $\Delta V_{it}$ ,  $\Delta N_{ot}$  and  $\Delta N_{it}$  versus TID and annealing

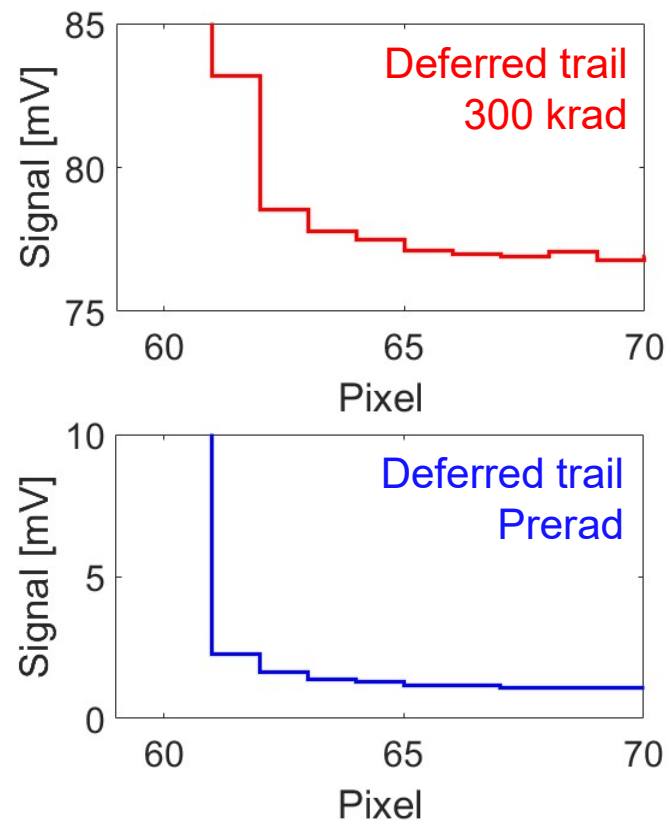
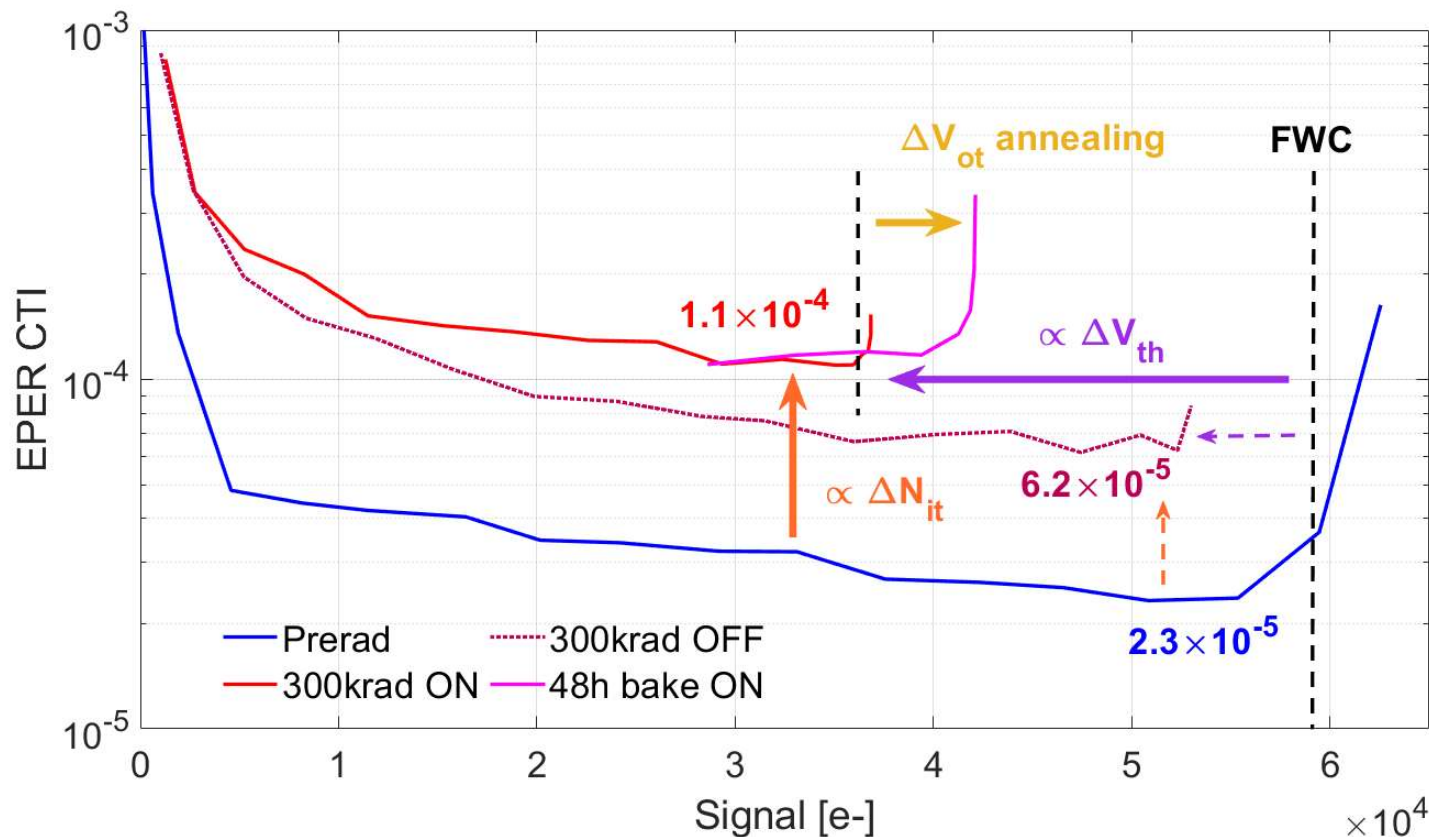


- Charge yield and space charge effects in the oxide are noticeable during irradiation.  $\Delta V_{ot}$  annealing is similar regarding both biasing, whereas  $\Delta V_{it}$  exhibits some reverse characteristics when grounded.



## 3 – Results

### Effects on CTI and FWC



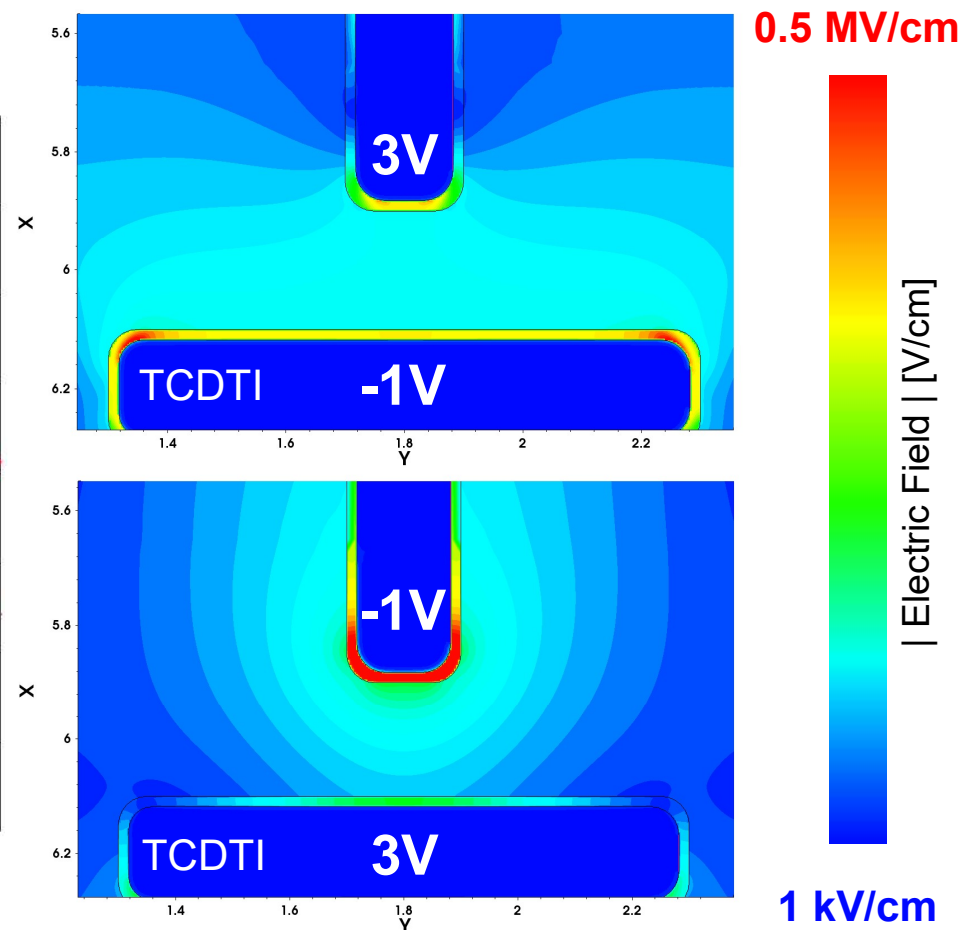
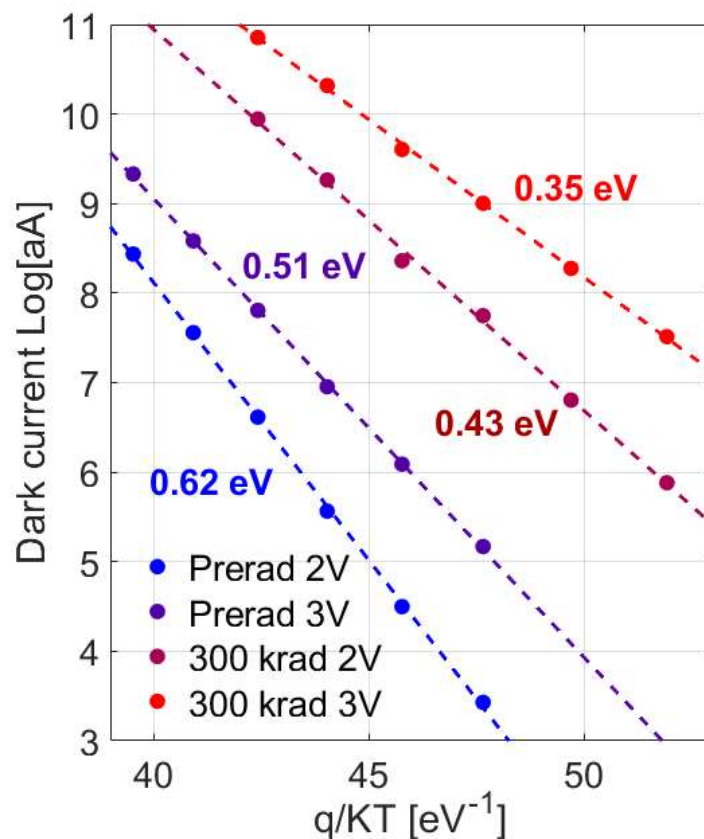
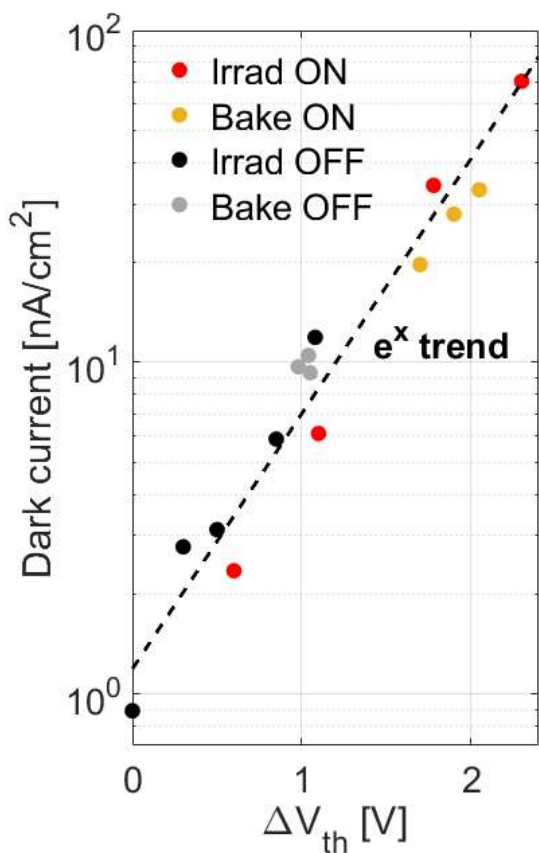
- FWC is reduced  $\propto \Delta V_{th}$  (no time for detrapping) and CTI is increased  $\propto \Delta N_{it}$ . Annealing restores mostly FWC through  $\Delta V_{ot}$  annealing (biased case). The OFF device is logically degraded in a lesser extent.





## 3 – Results

### Effects on Dark current



- Dark current exhibits an Electric field dependence with a reduced activation energy  $E_a$ . It originates from the surface potential difference yielded by two neighbour gates at  $V_{lo}$  and  $V_{hi}$  during charge transfer.



## 4 – Conclusion

### Takeaway notes

- A simple technique based on the properties of a Fully Depleted **CDTI-based CCD-on-CMOS** is successfully used to discriminate the role of **interface states ( $\Delta N_{it}$ )** and **oxide charges ( $\Delta N_{ot}$ )**.
- By exploring biasing conditions and annealing, TID effects on **Dark current, FWC and CTI** are correlated to the respective trap concentrations buildup.
- Up to **300 krad under worst case scenario**, **no critical Ionizing Dose effects are observed** :
  - The device takes profit of the CMOS intrinsic radiation hardness and of the MPP mode mitigating surface dark current.
  - Effects on FWC and Dark current can be partially reversed by adapting biasing.
  - ➔ Reducing further  **$E_{ox}$**  and **biases** is mandatory to yield the best performances.

*Biased during irradiation		This Work*	DG SOI MOSFET (FG)* [B. Jun <i>et al.</i> IEEE TNS 2004]	Rad-Hard CCD* [D. Burt <i>et al.</i> SPIE 2009]
$\langle \Delta V_{th} / \text{krad} \rangle$	$\langle \Delta V_{ot} / \text{krad} \rangle$	2.85	7.5	6
[mV/krad]	$\langle \Delta V_{it} / \text{krad} \rangle$	4.81		-
$\langle \text{Dark current} \rangle @RT$ [pA/cm <sup>2</sup> /krad]		5 (1μs transfer)	-	20

# Thank you for your attention

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Workshop on Radiation Effects on Optoelectronics and  
Photonics Technologies



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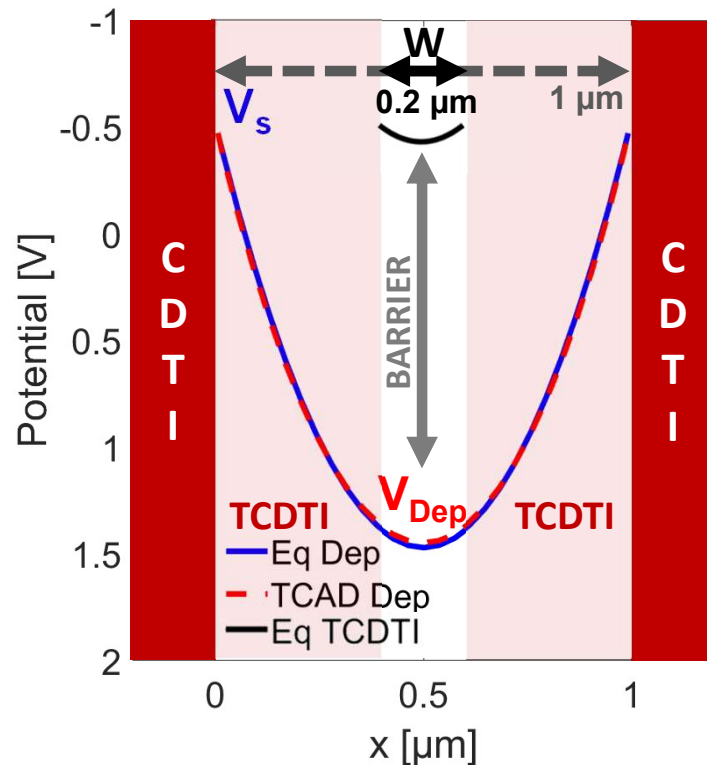
# Backup Slides

## 2 – Device Description

### CDTI based pixel

Parabolic potential well :

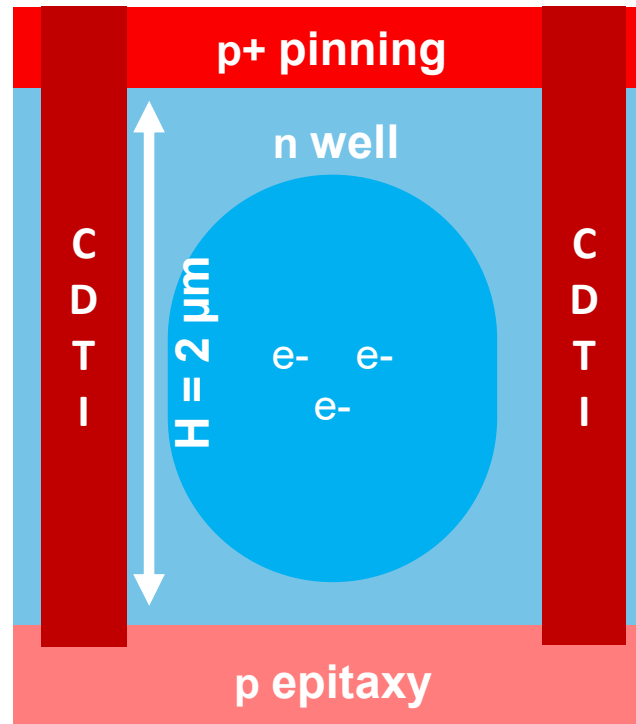
$$U(x) = \frac{-N_d q}{2\epsilon} (x^2 - Wx) + V_s$$



Antoine SALIH ALJ

Fully Depleted deep N-well  
Buried Channel :

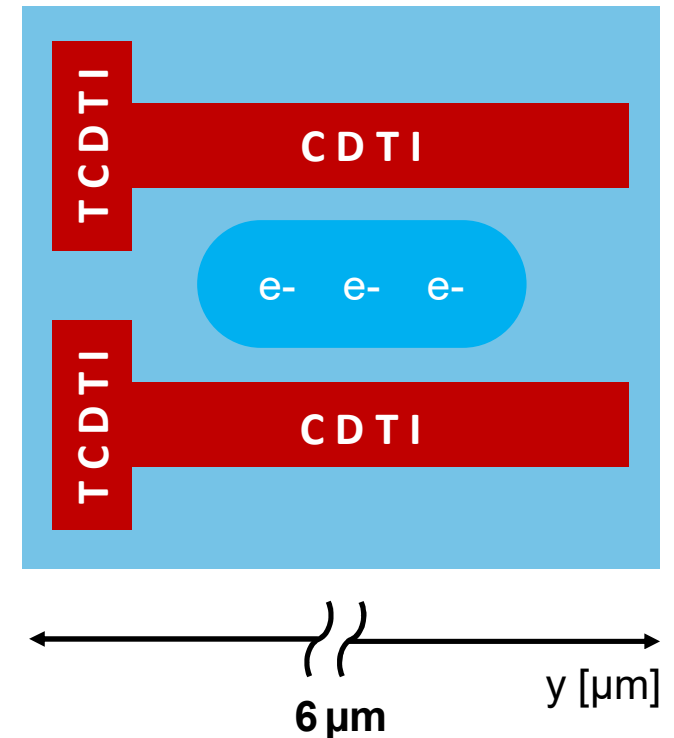
### Cross-section view



RADOPT 2023 – 29th-30th November 2023

Phase design and pitch :

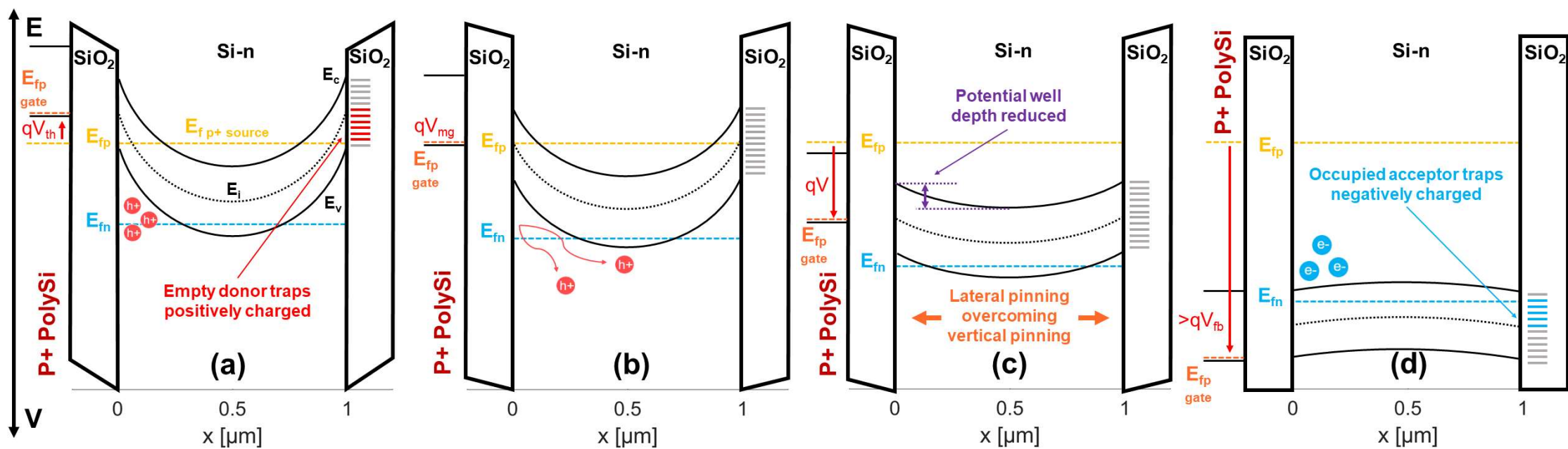
### Top view



13

## 2 – Device Description

### Band Diagram under full depletion

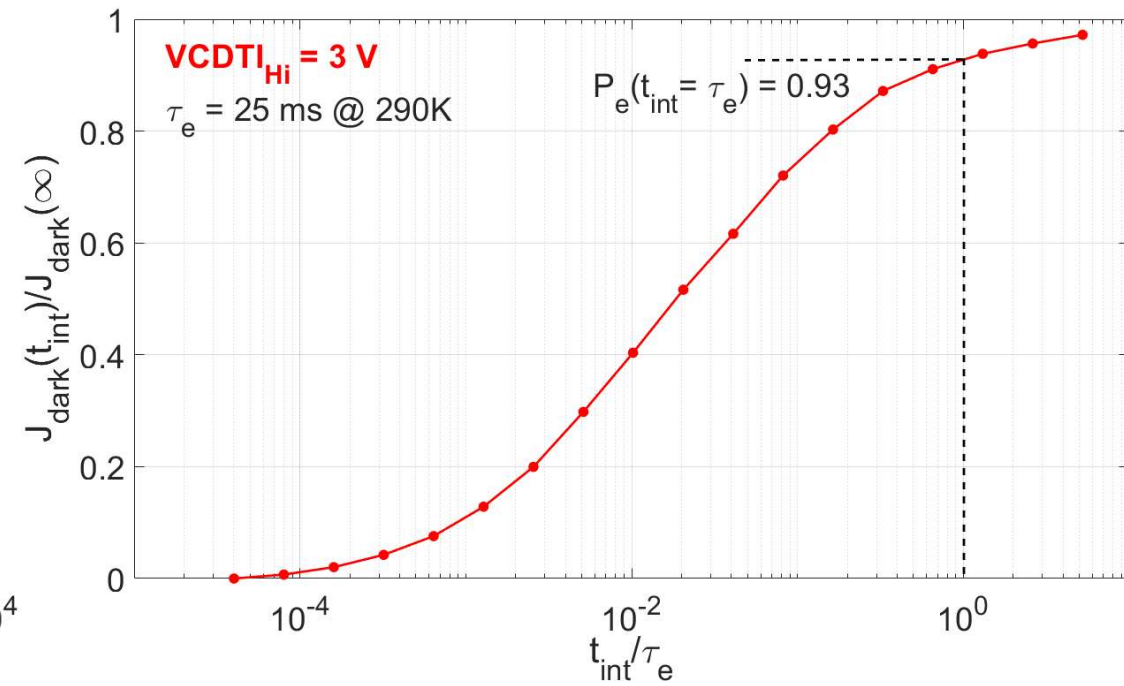
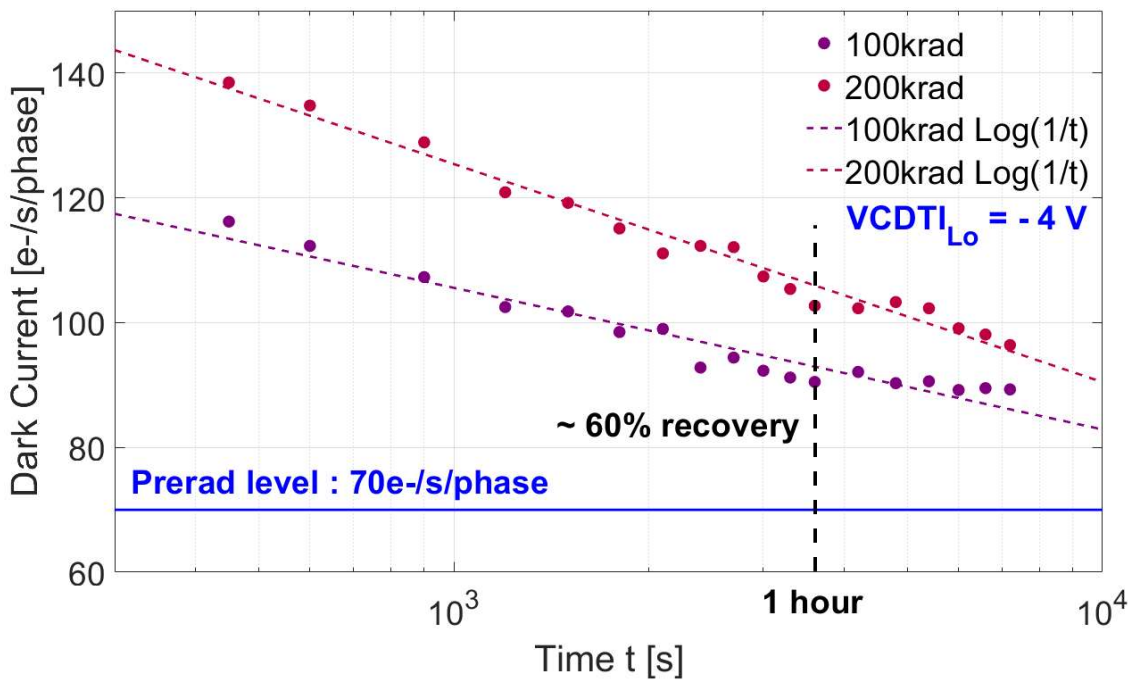


- The CCD is operated with interfaces inverted during storage and depleted during transfer. As a consequence, the interface trapped charge only fully contribute to the threshold voltage at inversion.



# 3 – Experimental Details

## RT Annealing & depletion dark current



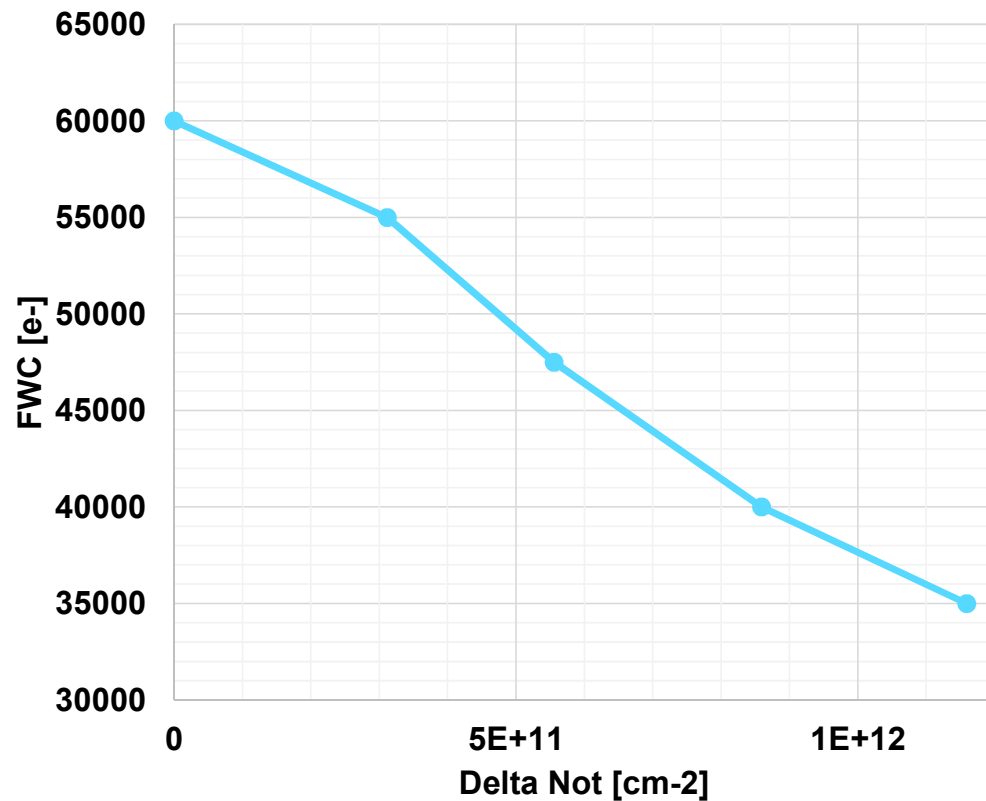
- RT annealing shows 60% dark current recovery after 1 hour. An other hour is needed for measurements, leaving two hours in between exposures (ESCC22900). Depleted dark current is steady after 2 to 3  $\tau_e$ .



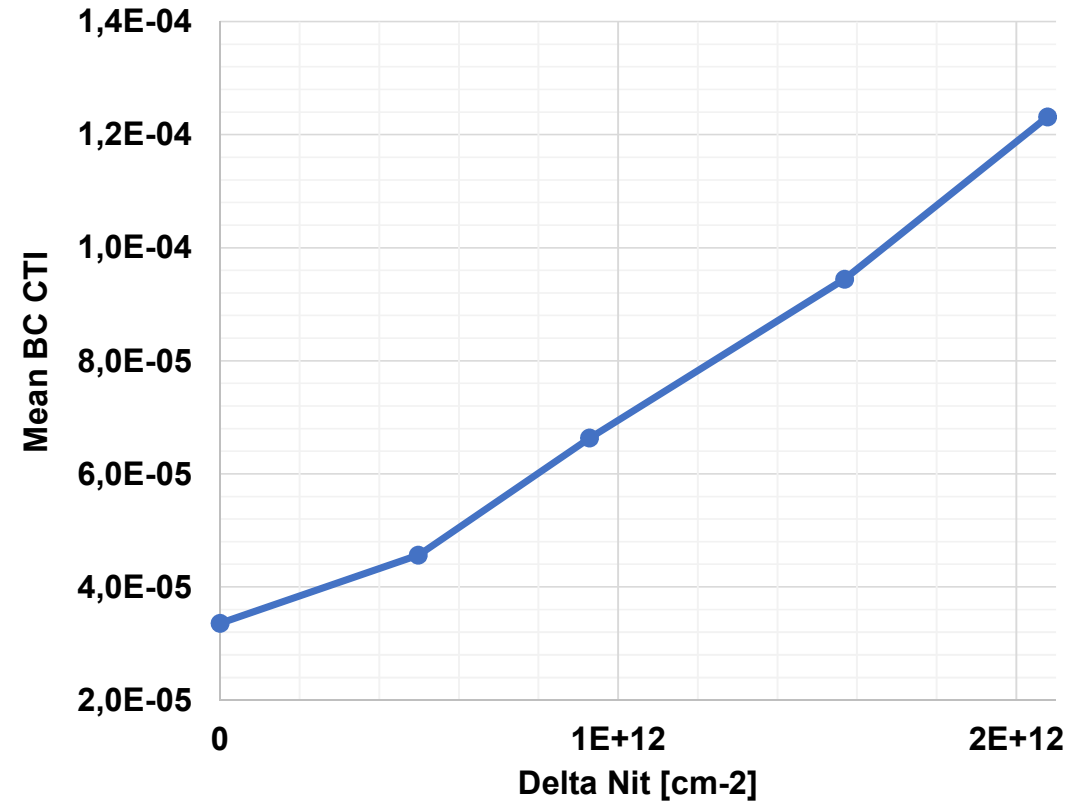
## 3 – Results

### Effects on CTI and FWC

- CTI : FWC vs Not**

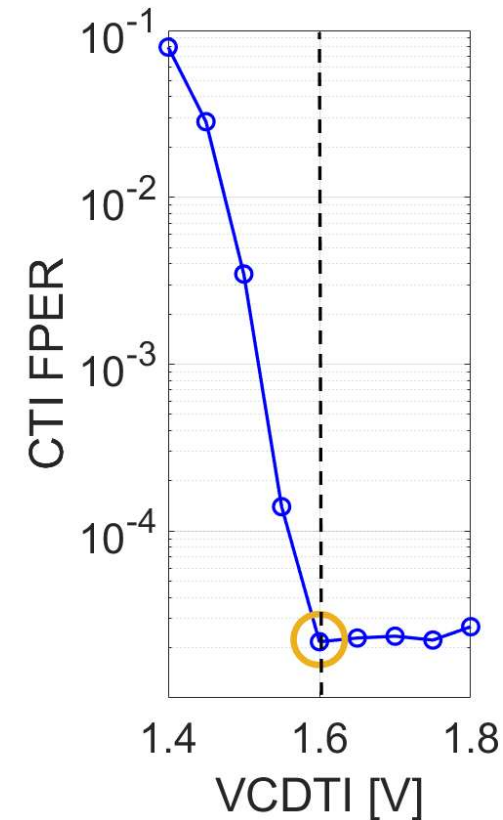
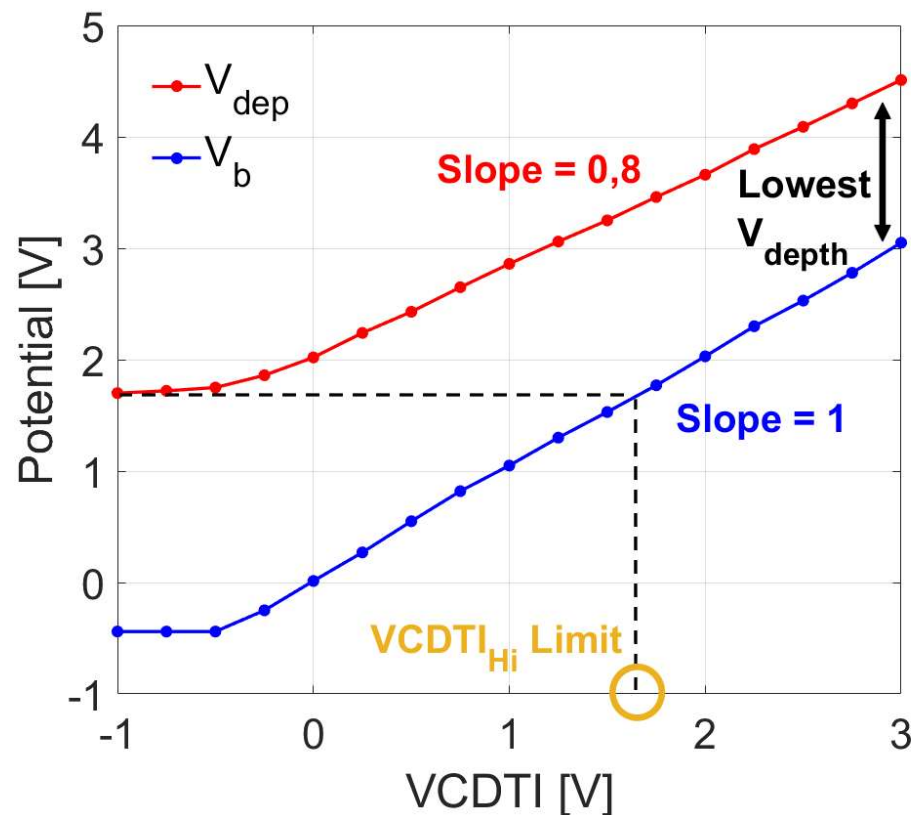


- CTI : CTI vs Nit**



## 2 – Device Description

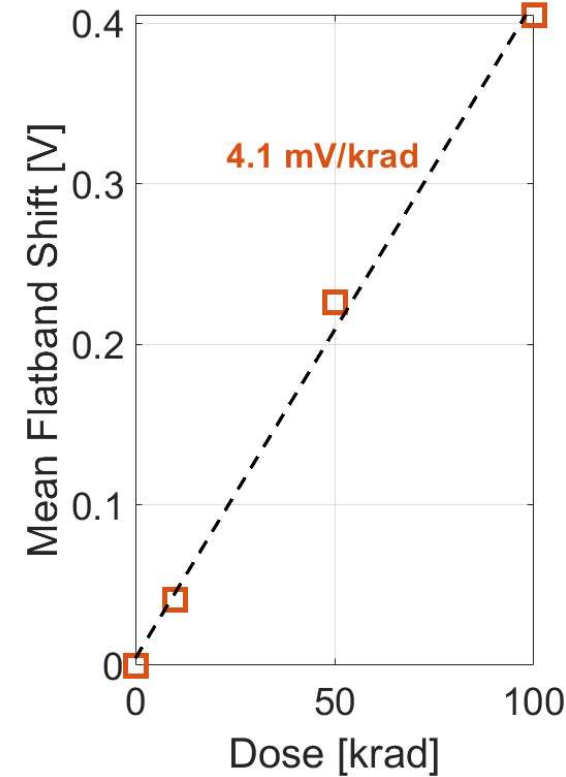
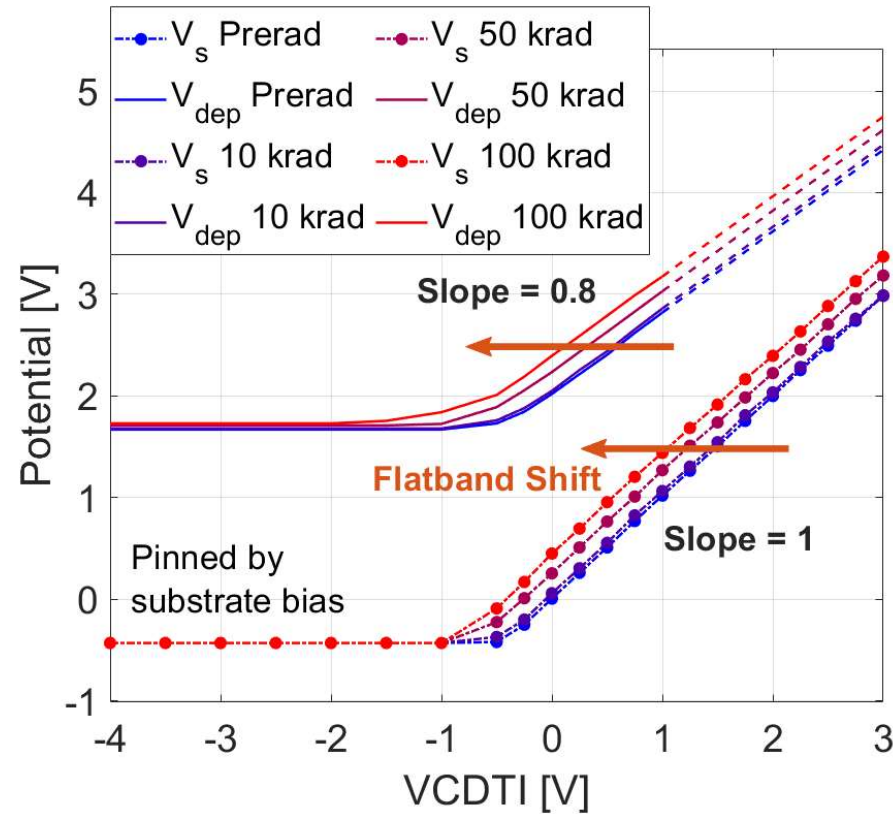
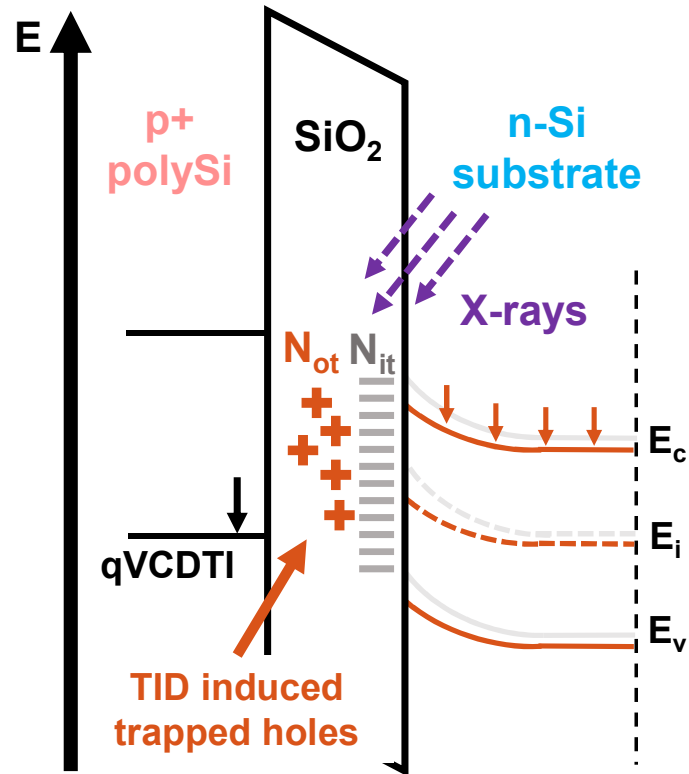
### Charge Transfer Operation



- 2-phase Multi-Pinned Phase (MPP) operation made possible by keeping all phases inverted during integration. The charge transfer operation requires a minimum  $VCDTI_{Hi}$  whose  $V_{depth}$  is dependant.

# 5 – Radiation Effects

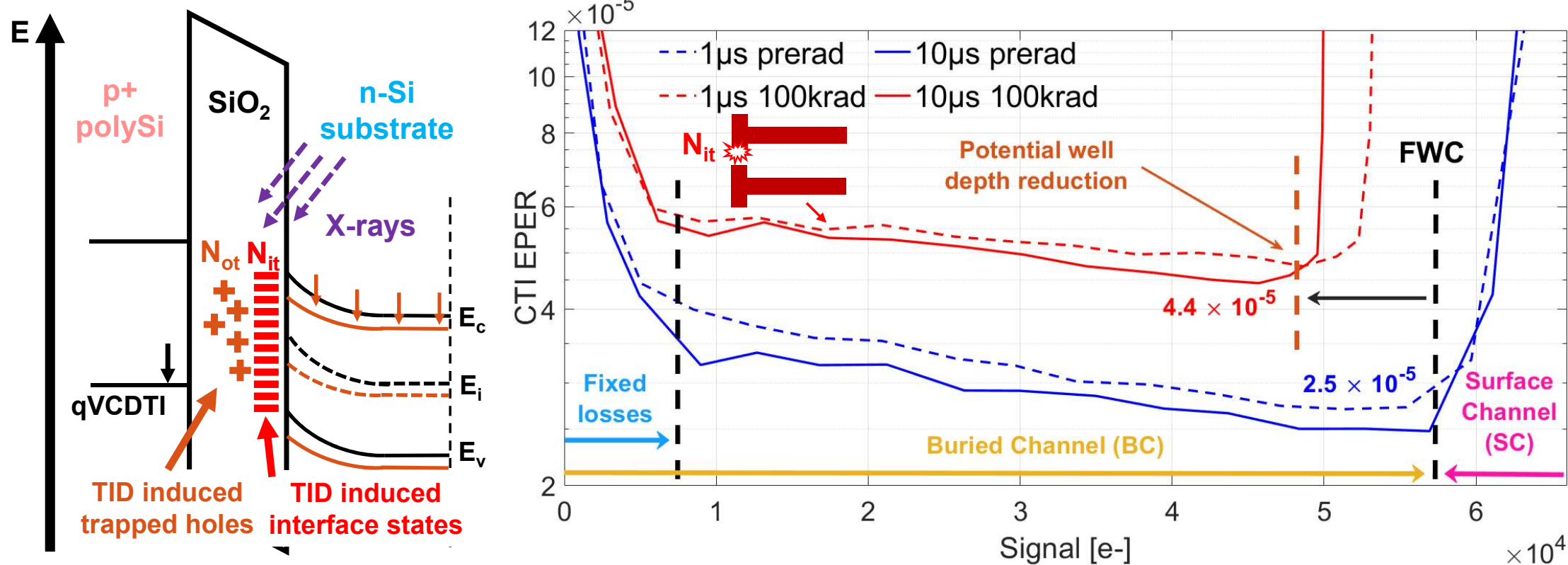
## TID – Flatband Shift



- TID induces a shift on the surface potential  $V_s$  which in turn shifts  $V_{dep}$ . The average value is 4.1 mV/krad.  $V_s$  and  $V_{dep}$  get closer as VCDTI increases meaning  $V_{depth}$  and FWC are reduced.

# 5 – Radiation Effects

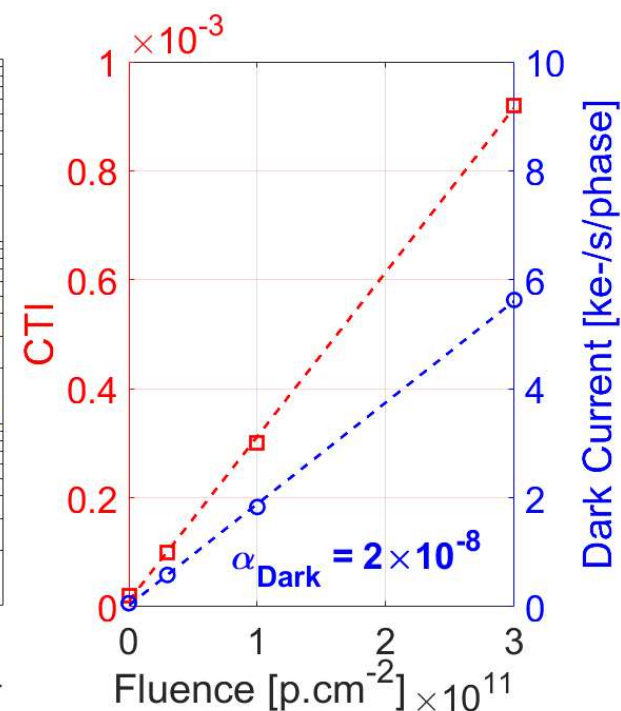
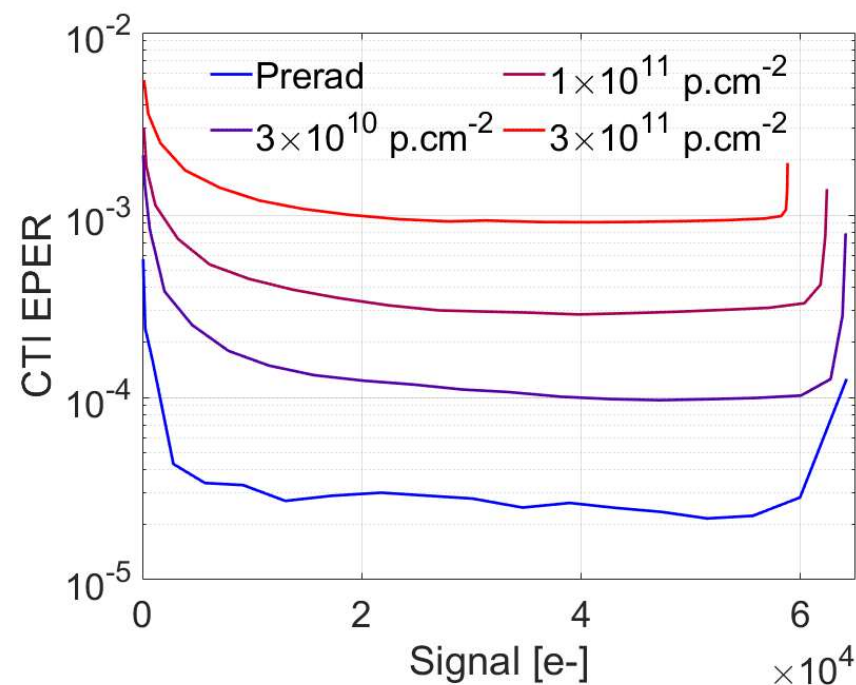
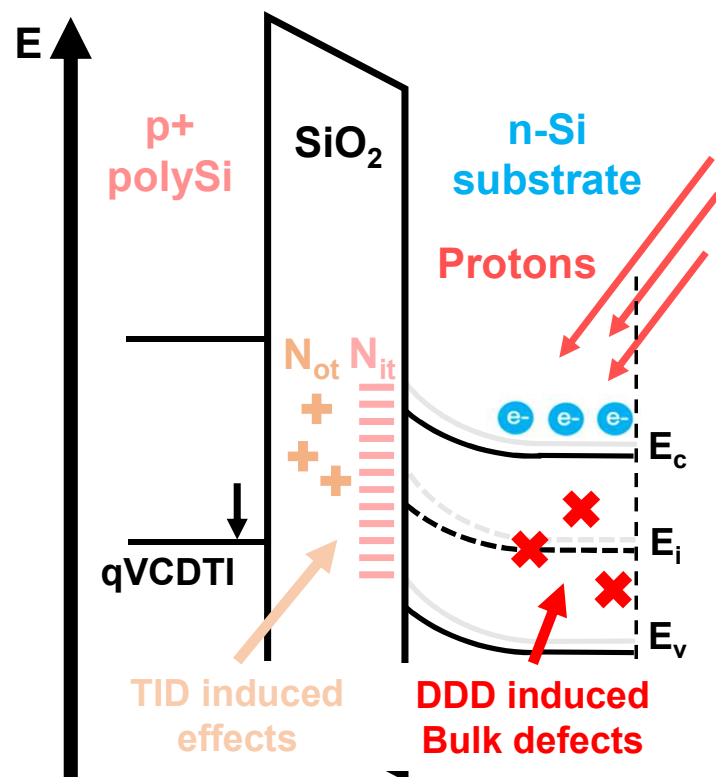
## TID – Charge Transfer Efficiency



- TID induces trapped holes in the oxide and interface traps buildup. The former causes a FWC reduction because of flatband shift. The later is responsible for a CTI deterioration, supposedly at the TCDTI level.

# 5 – Radiation Effects

## DDD - Displacement Damage Effects



$$K_{\text{Dark}} = \frac{\alpha_{\text{Dark}}}{V_{\text{dep}} N_{\text{IEL}_{62\text{MeV}}}} = 1.85 \times 10^5 \text{ e}^- \cdot \text{cm}^{-3} \cdot \text{sec per MeV} \cdot \text{g}^{-1}$$

- Protons induce defects in the Si bulk that are both responsible for a linear increase of Dark Current and CTI with respect to the Fluence. A  $K_{\text{dark}}$  close to the Universal Damage Factor is retrieved ( $1.9 \times 10^5$ ).